



FIG 3A

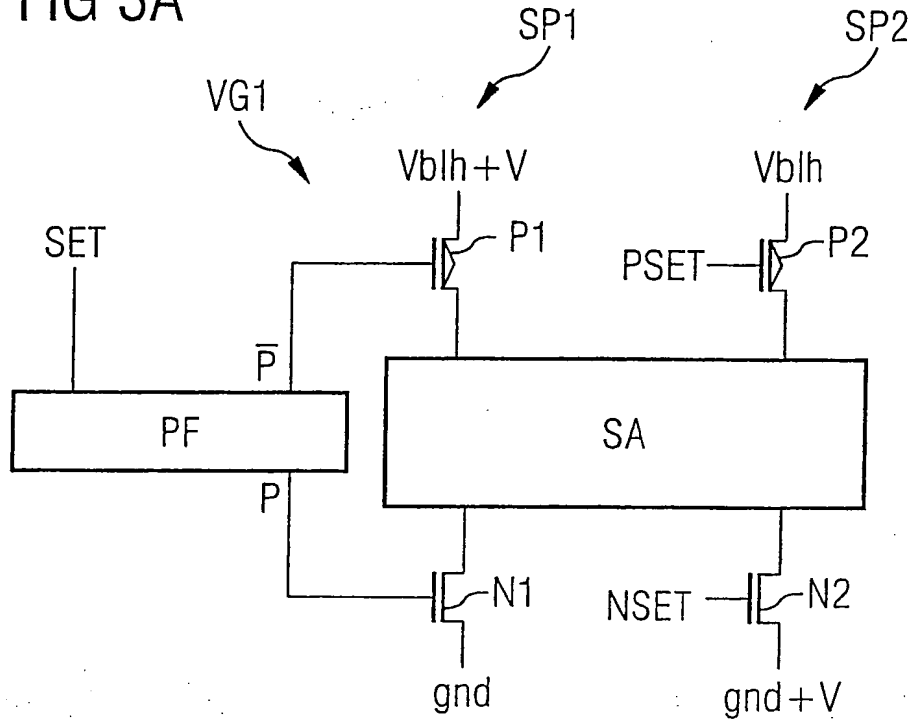


FIG 3B

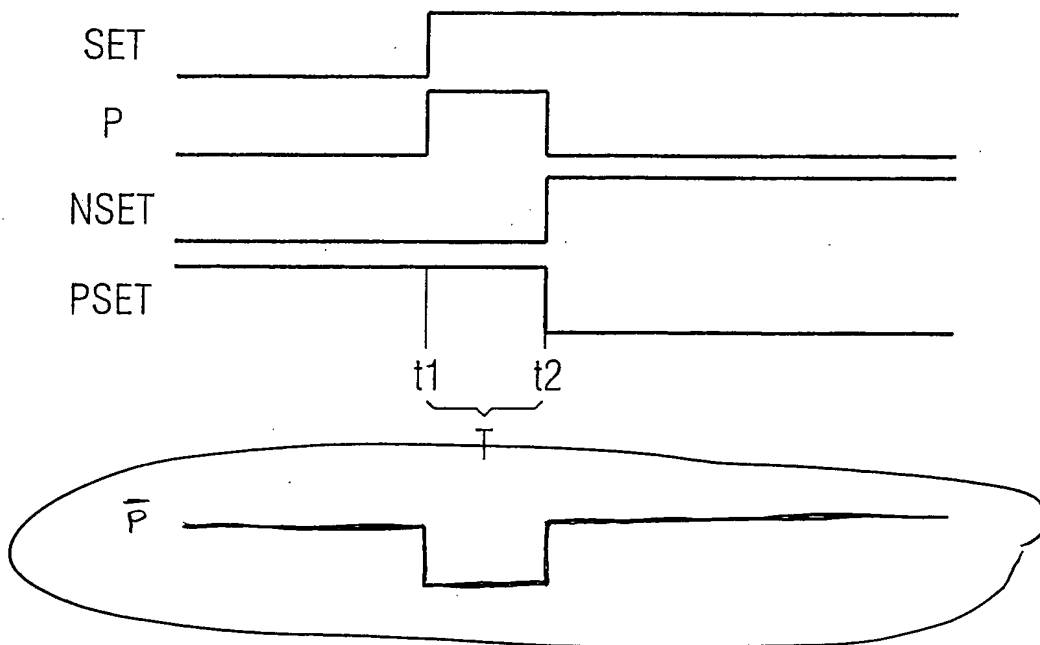


FIG 4A

The diagram shows a circuit element with two input blocks, PF and SA, and two output nodes, SP1 and SP2. The PF block has inputs SET, \bar{P} , and P. The SA block has inputs PSET and NSET. The circuit includes several transistors: P3 (PMOS, gate VG2, source $V_{blh}+V$, drain SP1), P4 (PMOS, gate V_{blh} , source SP1, drain SP2), P5 (PMOS, gate V_{blh} , source SP2, drain PSET), N3 (NMOS, gate $V_{blh}+V$, source gnd, drain SP1), N4 (NMOS, gate V_{blh} , source SP1, drain gnd+V), and N5 (NMOS, gate V_{blh} , source SP2, drain gnd+V). Two capacitors, C1 and C2, are connected between SP1 and gnd, and between SP2 and gnd+V, respectively. The PF block is connected to the gates of P3 and N3. The SA block is connected to the gates of P4 and N4. The SET input is connected to the gate of P3. The PSET input is connected to the gate of P5. The NSET input is connected to the gate of N5. The \bar{P} input is connected to the gate of P4. The P input is connected to the gate of N4. The $V_{blh}+V$ input is connected to the gate of P3. The V_{blh} input is connected to the gates of P4, P5, N4, and N5. The gnd and gnd+V inputs are connected to the sources of N3 and N5, respectively. The SP1 and SP2 outputs are connected to the drains of P3 and P4, and the sources of N4 and N5, respectively. The capacitors C1 and C2 are connected between SP1 and gnd, and between SP2 and gnd+V, respectively.